

# Workshop on Application Specific Processors - WASP 2003

## *Final Program*

8:30 – 8:40 **Welcoming Remarks**

8:40 – 10:00 **Session 1: *Application Specific Hardware Accelerators and Co-processors***  
Chair: Sanjay Patel (UI at Urbana-Champaign)

**Operating System Support for Interface Virtualisation of Reconfigurable Coprocessors,**  
M. Vuletic, L. Righetti, L. Pozzi, P. Ienne (*Swiss Federal Institute of Technology Lausanne*)

**A High Throughput AES-Based Programmable Crypto Coprocessor,**  
A. Hodjat, P. Schaumont, I. Verbauwhede (*UC Los Angeles*)

**A Fast, Low-Power Floating Point Unit for Multimedia (s),**  
C. Alvarez, M. Valero, J. Corbal, E. Salamí, J. A. R. Fonollosa (*UPC Barcelona*)

**An FPGA-based Search Engine for Unstructured Databases (s),**  
B. West, R. Indeck, R. Chamberlain, Q. Zhang (*Washington University*)

10:00 – 10:20 **Break**

10:20 – 12:00 **Session 2: *Clustering and Interconnect in Customizable Processors***  
Chair: Wayne Wolf (*Princeton*)

**Transformation Driven Power Reduction in Deep Sub-Micron Coupled Instruction Buses,**  
P. Petrov, A. Orailoglu (*UC San Diego*)

**Cost Sensitive Operation Partitioning for Synthesizing Custom Multicluster Datapath Architectures,**  
M. Chu, R. Ravindran, K. Fan, S. Mahlke (*U. of Michigan, Ann Arbor*)

**Analysis of the Performance of Coarse-Grain Reconfigurable Architectures with Different Processing Element Configurations,**  
N. Bansal, S. Gupta, N. Dutt, A. Nicolau (*UC Irvine*)

**Impact of Inter-cluster Communication Mechanisms on ILP in Clustered VLIW Architectures,**  
A. Gangwar, M. Balakrishnan, A. Kumar (*Indian Institute of Technology, Delhi*)

12:00 – 13:30 **Lunch**

13:30 – 14:20 **Keynote Speech:**

Chair: Daniel Gajski (*UC Irvine*)

Matthew Hatch, VP Advanced Systems Technology Group, ST Microelectronics

14:20 – 14:40 **Break**

14:40 – 16:25 **Session 3: Custom Architectures**

Chair: Siamak Arya (*Telairity Inc.*)

**The Hyperprocessor: a Template Architecture for Embedded Multimedia Applications,**

F. Karim, A. Mellan, B. Stramm (*ST Microelectronics*), T. Abdelrahman, U. Aydonat (*U. of Toronto*)

**Improving Application Performance by Dynamically Balancing Speed and Complexity in a GALS Microprocessor,**

G. Semeraro (*Rochester Institute of Technology*), D. H. Albonesi, S. Dropsho, G. Magklis, M. L. Scott (*U. of Rochester*)

**Asynchronous Event Handler Spawning using Communication Thread Cache,**

I. Kim (*USC*), Jean-Luc Gaudiot (*UC Irvine*), Jeffrey Draper (*USC*)

**Energy-Efficient Register Renaming in High-Performance Processors (s),**

J. L. Ayala, M. Lopez-Vallejo (*Universidad Politécnica de Madrid*), A. Veidenbaum (*UC Irvine*)

**A Novel Processor Architecture With Exact Tag-Free Pointers (s),**

M. Meyer (*University of Stuttgart*)

16:25 – 16:45 **Break**

16:45 – 18:00 **Panel: Future of Application Specific Processors: Issues and Challenges**

Organizer: Faraydon Karim (*ST Microelectronics*)

Panelists: Chris Rowen (*Tensilica*), JoAnn Paul (*CMU*), Peter Varman (*NSF*),  
Ramesh Chandra (*Qualcomm*), Naresh Soni (*ST Microelectronics*)